IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Canceled):

Claim 2 (Previously Presented): A digital magnetic recording/reproducing apparatus for recording and reproducing digital information comprising:

a Viterbi detector which decodes a signal sequence obtained by partial response equalization and produces n candidates of a decoded result, the candidates being a best candidate to an nth best candidate and being produced simultaneously by the Viterbi decoder;

an error detector which detects errors in the n candidates; and

an selector which selects from the candidates a candidate having no detected errors as a correct decoded result and supplies the correct decoded result to a recording decoder;

wherein the Viterbi decoder uses a path memory having a length which is shorter than a length of an error detection block used by the error detector.

Claim 3 (Previously Presented): A digital magnetic recording/reproducing apparatus according to claim 2, wherein the length of the error detection block is selected so that a coding rate after error detection is not less than 8/9.

Claim 4 (Previously Presented): A digital magnetic recording/reproducing apparatus according to claim 2, wherein the error detection block is a CRC (Cyclic Redundancy Check) block.

Claim 5 (Previously Presented): A digital magnetic recording/reproducing apparatus according to claim 2, wherein the Viterbi detector uses an LVA (List Viterbi Algorithm) for signal processing.

Claim 6 (Previously Presented): A digital magnetic recording/reproducing apparatus according to claim 2, further comprising a coder which adds error detection check bits to the signal sequence.

Claim 7 (Canceled):

Claim 8 (Previously Presented): A digital magnetic recording/reproducing method for recording and reproducing digital information comprising the steps of:

decoding a signal sequence obtained by partial response equalization and producing n candidates of a decoded result using a Viterbi decoder, the candidates being a best candidate to an nth best candidate and being produced simultaneously by the Viterbi decoder;

detecting errors in the n candidates; and

selecting from the candidates a candidate having no detected errors as a correct decoded result and supplying the correct decoded result to a recording decoder;

wherein the Viterbi decoder uses a path memory having a length which is shorter than a length of an error detection block used in the error detecting step.

Claim 9 (Previously Presented): A digital magnetic recording/reproducing method according to claim 8, wherein the length of the error detection block is selected so that a coding rate after error detection is not less than 8/9.

Claim 10 (Previously Presented): A digital magnetic recording/reproducing method according to claim 8, wherein the error detection block is a CRC (Cyclic Redundancy Check) block.

Claim 11 (Previously Presented): A digital magnetic recording/reproducing method according to claim 8, wherein the Viterbi detector uses an LVA (List Viterbi Algorithm) for signal processing.

Claim 12 (Previously Presented): A digital magnetic recording/reproducing method according to claim 8, further comprising the step of adding error detection check bits to the signal sequence.

Claim 13 (New): An apparatus for recording and reproducing digital information comprising:

a decoder which decodes a signal sequence and produces n candidates of a decoded result, each of the n candidates being divided into error detection blocks; and

a circuit which detects errors in the n candidates based on the error detection blocks, and selects a candidate having no errors from the n candidates as a correct decoded result,

wherein the decoder produces the n candidates using a path memory having a length which is shorter than a length of each of the error detection blocks.

Claim 14 (New): An apparatus according to claim 13, wherein the length of the error detection block is selected so that a coding rate after error detection is not less than 8/9.

Claim 15 (New): An apparatus according to claim 13, wherein the error detection blocks are CRC (Cyclic Redundancy Check) blocks.

Claim 16 (New): An apparatus according to claim 13, wherein the detector uses an LVA (List Viterbi Algorithm) for signal processing.

Claim 17 (New): An apparatus according to claim 13, further comprising a coder which adds error detection check bits to the signal sequence.

Claim 18 (New): A method for recording and reproducing digital information in a digital magnetic recording/reproducing apparatus, the method comprising:

decoding a signal sequence and producing n candidates of a decoded result, each of the n candidates being divided into error detection blocks;

detecting errors in the n candidates based on the error detection blocks; and

selecting a candidate having no errors from the n candidates as a correct decoded result,

wherein the n candidates are produced using a path memory having a length which is shorter than a length of each of the error detection blocks.

Claim 19 (New): A method according to claim 18, wherein the length of the error detection block is selected so that a coding rate after error detection is not less than 8/9.

Claim 20 (New): A method according to claim 18, wherein the error detection blocks are CRC (Cyclic Redundancy Check) blocks.